DIELECTRIC PROPERTIES OF OXIDIZED POROUS SILICON IN A LOW RESISTIVITY SUBSTRATE

Rebecca L. Peterson* and Rhonda F. Drayton

Department of Electrical and Computer Engineering, University of Minnesota,
200 Union Street Southeast, Minneapolis, Minnesota, 55455 USA; drayton@ece.umn.edu

***Abstract* — Oxidized porous silicon (OPS) is characterized for its high frequency electrical properties up to 50 GHz. Transmission line properties are determined from measurement data and are compared with high and low resistivity silicon benchmark designs. Best OPS performance of 50 Ohm lines is observed on oxide-capped OPS, having attenuation of approximately 2.93 dB/cm at 4 GHz with an effective dielectric constant of 3.25. This technology offers promise for extending the use of CMOS circuitry to higher RF frequencies.**

I. INTRODUCTION

Integration of high frequency passive components with CMOS circuitry is highly desirable. Wafer-level integration reduces interconnect length and complexity and lowers system size, weight and cost. Unfortunately, the divergent design requirements of active devices on low resistivity substrates and passive circuits on semi-insulating ones make their simultaneous implementation in CMOS-grade silicon very difficult. Researchers have attempted to circumvent this problem by using alternate dielectrics in multi-layer configurations such as spin-on polyimide [1] or by removing the lossy silicon substrate to form a suspended line [2], but these technologies are not CMOS compatible. Recent studies of coplanar waveguide lines on oxidized porous silicon (OPS) in low resistivity silicon, however, show promise with acceptable loss characteristics up to 20 GHz [3] using processes that could be integrated with standard CMOS processing [4].

High frequency passive circuit designs require knowledge of the effective dielectric constant as well as of the attenuation of the substrate. Moreover, the relationship between OPS fabrication techniques and these electrical properties needs to be elucidated so that material losses can be minimized and the dielectric constant accurately predicted. This paper presents the fabrication of OPS in low resistivity silicon and the characterization of finite ground coplanar waveguide transmission lines up to 50 GHz. The attenuation and effective dielectric constant are evaluated and OPS performance is compared to benchmark experimental data on low and high resistivity silicon.

II. FABRICATION AND DESIGN

Porous silicon is formed by anodization of single-crystal silicon at low current densities in a mixture of hydrofluoric acid (HF) and ethanol using the etch cell shown in the Fig. 1 schematic. The resulting material consists of nanometer-scale air columns in a fine network of crystalline silicon. The etch process and material morphology have been described in detail elsewhere [5]. Because of its interesting optical, thermal and structural properties, porous silicon has been proposed for use in a wide variety of applications over the last several decades [6] and is now being considered for high-speed RF applications.

For this work, p-type (Boron) <100> silicon wafers, 14 - 21 Ω-cm and 530 μm thick, are anodized at 10 mA/cm^2 in 49% HF:pure ethanol 5:3 for 29 minutes. The backside of the wafer is ion implanted and the implant is driven in to insure an ohmic contact from the secondary electrode to the wafer [5]. The resulting material has porosity of 56% (determined gravimetrically) and thickness of approximately 26 μm (determined by scanning electron micrograph in Fig. 2). Passivation is performed by rapid thermal oxidation (RTO) for 30 minutes at 350°C. Low oxidation temperatures are needed to terminate the dangling silicon bonds with oxygen without agglomeration of the silicon columns. Once coated with a few monolayers of oxygen, the material is chemically stable in ambient [5]. Some samples are capped with 4800Å of plasma-enhanced chemical vapor deposited (PECVD) silicon dioxide. Metal adhesion layers are evaporated and circuits are gold electroplated to 4 μm. Fig. 2 shows a cross-section of the material. Benchmark samples are made on bare low and high resistivity (n-type <100>, > 2000 Ω-cm, 525 μm thick) silicon wafers. Samples discussed in this paper are listed in Table I. Transmission lines have been designed using Hoffman's equations [7] and finite ground coplanar techniques [8].

* Ms. Peterson is now at the Department of Electrical Engineering of Princeton University, Princeton, New Jersey, 08544-5263 USA.

III. RESULTS

Device S-parameter response is measured using an HP8510C automatic network analyzer connected to a Cascade Microtech / Alessi RF1 microwave probing station equipped with Cascade Microtech GSG150 probes. Both probe-tip LRM (Line-Reflect-Match) and NIST's MultiCal [9] TRL (Through-Reflect-Line) calibrations are used. MultiCal TRL calibrations are performed separately for each wafer using on-wafer calibration standards.

A. Characteristic Impedance

Theoretically predicted [7] characteristic impedances for the measured lines are shown in Table II. The line dimensions, S-W-S_g=94-53-400 μm, are chosen for Z_0 equal to 50 Ω on silicon. On porous material the lower dielectric constant significantly increases Z_0.

B. Attenuation

Attenuation per unit length is calculated from measured S-parameter responses of 1.5 cm lines. These measurements are taken using an LRM calibration. Fig. 3 displays attenuation as a function of frequency and Table II contains data at selected frequency points.

The data given are total line attenuation. For the line dimensions and metallization used here, conductor attenuation is predicted to be quite low: 0.18-0.25 dB/cm at 4 GHz and 0.56-0.79 dB/cm at 40 GHz [7], where the range is for the spread of Z_0 (i.e. range of ε_{eff}) listed in Table II. For the low resistivity substrate cases, conductor attenuation is always a small fraction (<10%) of total attenuation. Hence, dielectric loss is assumed to be the primary cause of the total attenuation.

Low resistivity silicon exhibits attenuation a factor of 12 to 18 times greater than that of high resistivity silicon. The use of oxidized porous silicon reduces the total attenuation by at least 60% for frequencies up to 10 GHz. Further reduction of attenuation is limited by the non-50 Ω impedance of the OPS lines.

To demonstrate the effect of Z_0 on attenuation, a second set of 0.2 cm lines with S-W-S_g=100-20-400 μm is measured. The resulting data is found in Table III and Fig. 3. Conductor attenuation for these line dimensions is again predicted to be small: 0.28-0.45 dB/cm at 4 GHz; 0.45-0.71 at 10 GHz. Comparing data in Tables II and III, high resistivity substrate samples show a doubling of attenuation as Z_0 goes from 50 to 37 Ω. Conversely, for the OPS substrate at 4 GHz, the attenuation is reduced 39% from 4.81 to 2.93 dB/cm as the characteristic impedance changes from 70 to 52 Ω. Comparing 50 Ω lines at 4 GHz, the attenuation of OPS is only 3.7 times higher than the high resistivity benchmark.

Reference [3] reports results that are similar to ours (see Table III). In [3] a high temperature (1060°C) wet oxidation step was used to convert the OPS from a porous network of lossy silicon into a 20 μm thick SiO_2 layer. This conversion greatly reduces dielectric loss. However, such high temperatures generate mechanical stresses that can easily cause the OPS layer to peel or the wafer to bow [10]. This type of process is therefore usually limited to small areas as seen in [11]. Our process, in comparison, produces a continuous OPS region that is uniform over the majority of a 4-inch wafer surface (58 cm^2). Furthermore, attenuation of the OPS samples fabricated in this work is comparable to that produced with other (non-CMOS compatible) low resistivity silicon processes [1]-[2].

C. Effective Dielectric Constant

A simple volumetric approximation can be used to predict the relative dielectric constant of the porous material as

$$\varepsilon_{r,porous\_silicon} = \varepsilon_{r,silicon} \cdot (1-P) + \varepsilon_{r,air} \cdot (P) \qquad (1)$$

where $\varepsilon_{r,air}$ =1 and P is the porosity, or fraction of air in the porous silicon layer. When the porous silicon is capped with a PECVD oxide, a series capacitance model can be used to estimate the equivalent relative dielectric constant of the insulator stack:

$$\varepsilon_{r,eq} = \frac{\left(1+\frac{t_2}{t_1}\right)\cdot \varepsilon_1 \cdot \varepsilon_2}{\varepsilon_1 \cdot \frac{t_2}{t_1} + \varepsilon_2}. \qquad (2)$$

Here ε_1 and ε_2 are the relative dielectric constants of the two insulators, and t_1 and t_2 the respective layer thickness. The effective dielectric constant can be approximated as

$$\varepsilon_{eff} = \frac{(\varepsilon_r + 1)}{2}. \qquad (3)$$

Two sets of measured results and the predicted values of ε_{eff} are tabulated in Table IV. The effective dielectric constant as a function of frequency is given in Fig. 4.

Results from the three methods of determining ε_{eff} agree to within 5% for the bare silicon samples. As predicted, the dielectric constant is significantly reduced on OPS substrates. The relative dielectric constant drops from 11.7 for bare silicon to approximately 5.6 for PECVD-capped OPS. For the non-PECVD OPS sample, the values of ε_{eff} are intermediate as expected, but the measured results are significantly higher than the predicted value. In this case the metallization is not entirely planar but has penetrated the uncapped OPS layer. As a result, the electro-magnetic

fields are non-uniform and penetrate farther into the bulk silicon below the OPS. The strong contribution of this high index substrate degrades the electrical response. The addition of the PECVD capping layer eliminates this problem, as is shown by the excellent agreement (to within 5%) between the measured and predicted ε_{eff} values, and by the lower attenuation noted earlier.

IV. Summary

Oxidized porous silicon has proven to be a promising RF-microwave material. It offers good attenuation characteristics with low ε_{eff} over large areas on low resistivity silicon wafers, in a process that is amenable to CMOS integration. The moderate attenuation is of the order of high resistivity silicon loss, and can be further reduced by increasing the porosity, increasing the OPS layer thickness [4], or improving the loss characteristics of the capping layer. The low ε_{eff} also supports results shown for integrated inductors [12] and offers new possibilities for integrating distributed passive elements into CMOS circuits.

Acknowledgements

The authors acknowledge the support of Prof. Stephen Campbell and Dr. Greg Cibuzar of the MicroTechnology Laboratory, the laboratory assistance of Isaac Itotia and Jeremy Haley at the University of Minnesota, as well as initial discussions with Rebecca Welty at University of California, San Diego, and the technical advice on porous silicon of Professor Phillipe Fauchet and Dr. Selena Chan at University of Rochester, NY. This work has been supported by a National Science Foundation Graduate Fellowship[1] and an Automatic RF Techniques Group (ARFTG) Microwave Measurement Student Fellowship.

References

[1] B.-K. Kim, B.-K. Ko, K. Lee, J.-W. Jeong, K.-S. Lee, and S.-C. Kim, "Monolithic planar RF inductor and waveguide structures on silicon with performance comparable to those in GaAs MMIC," *International Electron Devices Meeting (IEDM) 1995*, pp. 717-720, 1995.

[2] V. Milanović, M. Gaitan, E. D. Bowen, and M. E. Zaghloul, "Micromachined microwave transmission lines in CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 5, pp. 630-635, May 1997.

[3] C.-M. Nam, and Y.-S. Kwon, "Coplanar waveguides on silicon substrate with thick oxidized porous (OPS) layer," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 11, pp. 369-371, November 1998.

[4] R. J. Welty, S. H. Park, P. M. Asbeck, K.-P. S. Dancil, and M. J. Sailor, "Porous silicon technology for RF integrated circuit applications," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Ann Arbor, Michigan, USA, pp. 160-163, September 17-18, 1998.

[5] A. Halimaoui, "Porous silicon: material processing, properties and applications," in *Porous Silicon Science and Technology*, eds. J.-C. Vial and J. Derrien, New York: Springer-Verlag, pp. 33-52, 1995.

[6] L. T. Canham, *Properties of Porous Silicon*, London: Institute of Electrical Engineers (UK), 1996.

[7] R. K. Hoffman, *Handbook of Microwave Integrated Circuits*, Norwood, MA: Artech House, Inc., 1987.

[8] K. J. Herrick, "W-band three-dimensional integrated circuits utilizing silicon micromachining," PhD thesis, Dept. of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, 2000, Chapters 1-2.

[9] R. Marks, "A multiline method of network analyzer calibration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 7, pp. 1205-1215, July 1991.

[10] Y.-H. Xie, M. R. Frei, A. J. Becker, C. A. King, D. Kossives, L. T. Gomez, and S. K. Theiss, "An approach for fabricating high-performance inductors on low-resistivity substrates," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 9, pp. 1433-1438, September 1998.

[11] C.-M. Nam and Y.-S. Kwon, "Selective oxidized porous silicon (SOPS) substrate for microwave power chip-packaging," in *IEEE 5th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP '96)*, Napa, CA, USA, pp. 202-204, October 28-30, 1996.

[12] C.-M. Nam and Y.-S. Kwon, "High-performance planar inductor on thick oxidized porous silicon (OPS) substrate," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 8, pp. 236-238, August 1997.

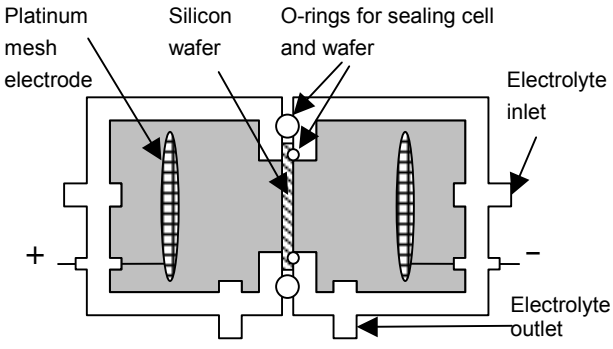
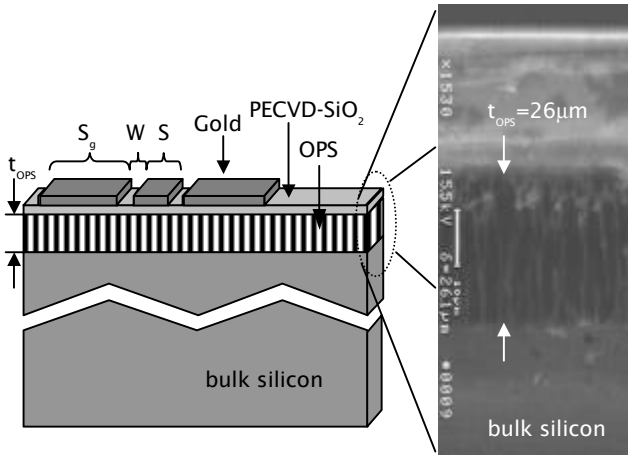


Fig. 1. Schematic of porous silicon etch cell

[1] Any opinions, findings, conclusions or recommendations expressed in this publication are those of the authors and do not necessarily reflect the views of the National Science Foundation.



(a) (b)

Fig. 2. (a) Schematic of finite ground coplanar transmission line cross-section on PECVD-capped OPS (not to scale) (b) Scanning electron micrograph (x1530) of 26 μm oxidized porous silicon, rapid thermally oxidized at low temperature and capped with 0.48 μm PECVD oxide.

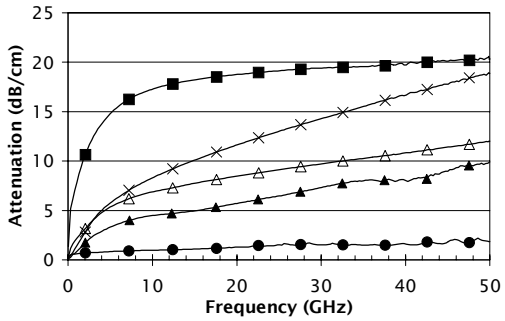


Fig. 3. Attenuation (dB/cm) as a function of frequency for various lines. Solid markers indicate lines with characteristic impedance near 50 Ω. Legend:

solid square (■) 50 Ω on low rho
solid circle (●) 50 Ω on high rho
letter x (X) 63.0 Ω on OPS + RTO (Fig. 3 only)
asterik (∗) 39.7 Ω on OPS + RTO (Fig. 4 only)
open triangle (Δ) 69.9 Ω on OPS + RTO / PECVD
solid triangle (▲)52.1 Ω on OPS + RTO / PECVD (Fig. 3 only)

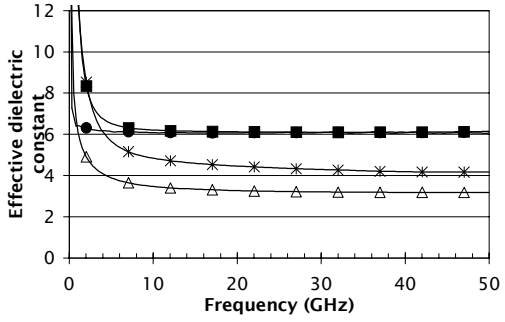


Fig. 4 Effective dielectric constant as a function of frequency from MultiCal TRL calibration output. See Fig. 3 legend for symbol definitions.

TABLE I
EXPERIMENTAL SAMPLES

Sample	Substrate	Dielectric	Metal
low rho	p-type silicon ρ =14-21 Ω-cm	none	Gold 4 μm
high rho	n-type silicon ρ >2 k Ω-cm	none	"
OPS + RTO	p-type silicon ρ =14-21 Ω-cm	26 μm porous silicon of 56% porosity, rapid thermally oxidized	"
OPS + RTO / PECVD	p-type silicon ρ =14-21 Ω-cm	26 μm porous silicon of 56% porosity, rapid thermally oxidized and capped with 0.48 μm PECVD SiO_2	"

TABLE II
ATTENUATION (dB/cm) AT SELECTED FREQUENCIES FOR LINES WITH S-W-S_G = 94-53-400 μm, L=1.5 cm

Sample	Predicted Z_0 [7]	Total measured attenuation in dB/cm			
		4 GHz	10 GHz	20 GHz	40 GHz
low rho	50.0 Ω (ε_{eff}=6.35)	13.83	17.28	18.76	19.88
high rho	50.0 Ω (ε_{eff}=6.35)	0.80	0.98	1.32	1.63
OPS + RTO	63.0 Ω (ε_{eff}=4.00)	5.07	8.32	11.64	16.75
OPS + RTO / PECVD	69.9 Ω (ε_{eff}=3.25)	4.81	6.89	8.48	10.78

TABLE III
ATTENUATION (dB/cm) AT SELECTED FREQUENCIES FOR LINES WITH S-W = 100-20 μm, L=0.2 cm

Sample	Predicted Z_0 [7]	Total measured attenuation in dB/cm	
		4 GHz	10 GHz
Reference [3]	59.4 Ω (ε_{eff}=2.50)	1.08	3.26
high rho	37.2 Ω (ε_{eff}=6.35)	1.69	1.83
OPS + RTO / PECVD	52.1 Ω (ε_{eff}=3.25)	2.93	4.50

TABLE IV
EFFECTIVE DIELECTRIC CONSTANT
(A) CALCULATED FROM MEASURED TRANSMISSION LINE PHASE (B) MULTICAL TRL CALIBRATION OUTPUT
(C) PREDICTED USING FORMULAE (1)-(3)

Sample	(A) ε_{eff} measured phase	(B) ε_{eff} at 50 GHz measured with MultiCal	(C) ε_{eff} predicted
low rho	6.05	6.14	6.35
high rho	6.14	6.06	6.35
OPS + RTO	3.99	4.17*	3.35
OPS + RTO / PECVD	3.25	3.18	3.33

* This TRL used calibration standards with S-W-S_g = 167-17-400μm. All other data are from lines with S-W-S_g = 94-53-400 μm.